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Nanopatterning of oxide 2-dimensional electron systems using low-temperature ion milling

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Abstract

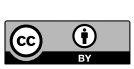
We present a 'top-down' patterning technique based on ion milling performed at low-temperature, for the realization of oxide two-dimensional electron system devices with dimensions down to 160 nm. Using electrical transport and scanning Superconducting QUantum Interference Device measurements we demonstrate that the low-temperature ion milling process does not damage the 2DES properties nor creates oxygen vacancies-related conducting paths in the STO substrate. As opposed to other procedures used to realize oxide 2DES devices, the one we propose gives lateral access to the 2DES along the in-plane directions, finally opening the way to coupling with other materials, including superconductors.

Keywords: oxide 2DES, nanodevices, oxide field effect devices

(Some figures may appear in colour only in the online journal)

1. Introduction

The wealth of properties shown by transition metal oxide materials has stimulated in the latest years an intense research into oxide heterostructures, where such properties can be modulated via structural, chemical or electronic coupling [1]. Interfaces between different complex oxides, in particular, give rise to extraordinary and unexpected phenomena. At the $LaAlO_3/SrTiO_3$ (LAO/STO) interface, for example, a superconducting, highly tunable two-dimensional electron system (2DES) develops [2]. This system can also be engineered to obtain even more intriguing multi-functional heterostructures. Introducing a magnetic $EuTiO_3$ layer between LAO and STO, for instance, a spin-polarized, superconducting oxide 2DES can be realized [3, 4]. Using Ca-doped STO substrates ferroelectricity can be added to the rich phase diagram of LAO/STO [5, 6]. The relevance of oxide 2DES for possible electronic applications is also emerging [7–9]. Experiments show that oxide 2DES can be used to perform spin-to-charge conversion with high efficiency [10], are suitable for transistor [11, 12], photonic and high frequency applications [13, 14]. These are some of the reasons for the recent interest in the realization of oxide based nanodevices, which could give the unique opportunity of investigating the physics of a 2D system in detail and



studying the interaction among several, in some cases antithetical, electronic phases.

In the latest years, several techniques have been used to realize nanodevices based on novel materials for advanced electronic applications, from ultra-high resolution electron beam lithography to direct writing using electron beams [15]. Specific device fabrication techniques were also developed soon after the discovery of the LAO/STO system. Scanning a voltage-biased metallic tip of an atomic force microscope (AFM) over the surface of a 3 unit cell (u.c.) thick LAO film enables to locally 'write' conducting channels at the interface, with a lateral resolution down to 2 nm [16–18]. A second approach is based on the realization of a pre-patterned substrate. Photo- or electron-beam lithography is used to define a resist mask reproducing the desired devices layout, which is then transferred to the STO substrate via deposition of an amorphous oxide layer and lift-off. Subsequently, the LAO film is deposited creating a conducting interface on the areas not covered by the amorphous template [19, 20]. A third patterning method is based on low-energy Ar ion beam irradiation of the LAO/STO interface [21]. The LAO/STO sample is firstly covered with a resist mask, then Ar irradiation eliminates the electrical conductivity at the interface in the exposed areas, without physical removal of the LAO film.

Thanks to the techniques described above, great progress has been made in the understanding of oxide interface physics. However, many issues are still open. The nature of the superconducting ground state in the LAO/STO system, for example, is still not completely understood. Several theoretical [22–25] and experimental [18, 26, 27] works indicate an unconventional superconducting ground state for this 2DES, but a final proof of the superconducting order parameter symmetry is still lacking. A direct way to probe the order parameter symmetry would be to couple the 2DES with a conventional superconductor, as for example has been done to study the order parameter symmetry of high temperature superconductors (HTS) [28]. In the case of oxide interfaces having intrinsic 2D nature, this coupling should take place in the in-plane directions. The nanofabrication techniques currently available, on the other hand, result in devices where the 2DES patterned channels are encapsulated in a crystalline or amorphous matrix, making it very difficult to perform such lateral electrical transport experiments.

In this work we present oxide 2DES nanodevices realized with a technique based on low-temperature ion milling, which allows to expose the sides of the nanostructures. Ion milling is commonly used for patterning of complex devices but, when applied to oxide materials, it can promote thermally activated oxygen desorption. In our case, this could lead to the formation of conducting areas in the STO substrate and electrical shorts between the devices [29]. We demonstrate that the careful tuning of the milling parameters and the cooling of the sample during the milling process (as sometimes done for the preparation of samples for transmission electron microscopy [30]) greatly limits the substrate damage. Our process results in nanodevices down to 160 nm in width. The absence of conducting paths in the substrate is clearly demonstrated by the transport properties of the devices and using scanning Superconducting QUantum Interference Device (SQUID) measurements. Moreover, the STO areas exposed after the ion-milling show very ordered terrace structures, therefore they could host the growth of complex materials laterally coupled to the oxide 2DES.

2. Methods

In this work we present the properties of devices based on $LaAlO_3/EuTiO_3/SrTiO_3$ (LAO/ETO/STO) heterostructures [4]. However, the fabrication procedure we describe is suitable also for LAO/STO and whatever type of oxide thin film and interface. The process is illustrated in panels (a)–(c) of figure 1. Initially, LAO(10 u.c)/ETO(2 u.c.) heterostructures (panel (a)) are realized by pulsed laser deposition on TiO_2-terminated (001) STO substrates. A KrF excimer laser (wavelength 248 nm, pulse rate 1 Hz) is focused on a sintered $Eu_2Ti_2O_7$ or on a crystalline LAO target at a fluency of 1.3 J cm^{-2}. During the deposition the substrate is kept at 680°C in oxygen partial pressure p_{O_2} of 1×10^{-4} mbar. The layer by layer thin films growth is monitored using reflection high-energy electron diffraction (RHEED). Following deposition, the sample is slowly cooled down to room temperature in $p_{O_2} = 1 \times 10^{-4}$ mbar [3].

After deposition of the heterostructures, a resist mask is realized using photolitography or electron beam lithography (figure 1(b)). In the latter case, we use a layer of negative tone ma-N2403 electron beam resist from Micro Resist Technology GmbH, with a thickess of 200 nm [31].

After resist development, the LAO/ETO areas not protected by the mask are etched with a low-intensity Ar ion milling process. We use a beam current of 8 mA and a beam voltage 400 V for a 3 cm beam aperture. These parameters result in a stable etching rate of 2 nm min^{-1} for the oxide layers, and the LAO/ETO areas not protected by resist are removed in 3 min of milling. The thickness of the resist mask ensures that the areas covered by the resist are well protected throughout this brief ion milling process. During the process the sample is glued on a cold finger kept at low temperature (−150 °C). This approach has been used in the past to realize nanoscale biepitaxial HTS grain boundary junctions and devices [32–34]. It was found that cooling the sample during the ion milling is crucial to ensure minimal loss of oxygen from the oxide HTS film, especially in the grain boundary areas.

After transferring the resist geometry to the oxide layers, the mask is finally washed away in an acetone bath (figure 1(c)). After fabrication, all the devices are inspected by atomic and lateral force microscopy using an AFM PARK 100 instrument in contact mode (force 15 nN, tip nanosensor NC36 model).

The transport properties of the devices were tested down to 5 K using a variable temperature cryostat. In order to compare the electrical transport properties of devices with different dimension and geometry, the sheet resistance value $R_{sheet} = R * f$ (with f a shape factor related to the device

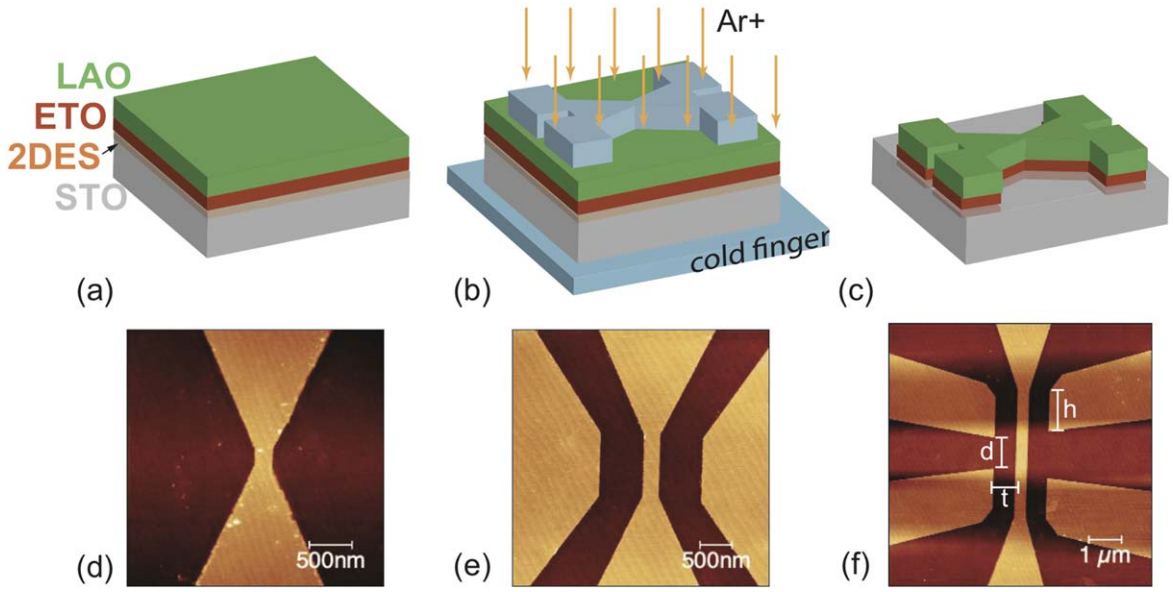


Figure 1. Sketch of devices fabrication process and contact mode AFM topography images of some of the LAO/ETO/STO devices realized. After the ETO/LAO bilayer is deposited (a), a resist mask is realized via photo or electron beam lithography and low temperature ion milling is used to remove the exposed areas of the ETO/LAO bilayer (b). Finally, the resist is washed away in an acetone bath (c). In the lower part of the figure we show the AFM images of a Dayem bridge (d), a side gate device with one pair of lateral electrodes (geometry 1S) (e) and a side gate device with two pairs of lateral electrodes (geometry 2S) (f).

geometry) can be used as a reference. In order to calculate the factor f for complex geometries, we perform finite element simulations using COMSOL MULTIPHYSICS software, as described in [12, 35]. Hall effect was tested applying a perpendicular magnetic field in a Physical Properties Measurement System (PPMS Quantum Design) and an Oxford Instruments-MagLab magnetometer. Finally, the spatial distribution of the current flow was mapped using a scanning SQUID microscope.

3. Results

Figures 1(d)–(f) show representative AFM images of devices realized using e-beam lithography: a constriction (Dayem bridge) with width $w = 200$ nm and length $L = 160$ nm (d), a side gate device with one pair of lateral electrodes (geometry 1S) with a central channel 250×1000 nm (e) and a side gate device with two pairs of lateral electrodes (geometry 2S) and a central channel 350×4000 nm (f). Well defined patterns with sharp edges are clearly visible, as well as the terraces on the LAO/ETO bilayer replicating those on the underlying substrate. In order to characterize the surface of etched devices we show in figure 2 contact mode AFM and lateral force microscopy images acquired in smaller regions of one of the Dayem bridge devices. Panel (a) shows that, remarkably, the terraces structure is preserved in the ion-milled areas of the substrate, as it can be seen also from the steps in the line profile of panels (c) and (f). The step height of each terrace is 3.9 Å (panel (f)). Panels (b) and (e) show that the lateral force signal is the same on each consecutive terrace, suggesting single atomic termination. Small inhomogeneities in the topographic and lateral force microscopy (2–5 nm wide, less than one unit cell high) on a single terrace are related to native defects present on the STO single crystal surface before the deposition (imperfect TiO_2 termination) [36] or in the LAO surface, common also to LAO/STO samples [37]. The data shown in figures 1 and 2 demonstrate that the ion milling process causes minimal structural damage to the exposed STO surfaces.

All the devices show a metallic behavior, as for example reported for a Dayem bridge in figure 3(a). In the inset we show the R_{sheet} as a function of devices dimensions. We include data from a large sample (500×500 μm) realized resorting to photolithography followed by low-temperature ion milling. Its properties are comparable to those of pristine (no patterned) heterostructures.

In [38] LAO/STO nanochannels were realized using a BCl_3-based reactive ion-etching process. The authors find that the R_{sheet} increases with decreasing width and infer a sidewall depletion of 20 ± 3 nm on each side of the structures. From the inset of figure 3(a) it can be seen that, in our case, R_{sheet} is approximately constant with the device width, and similar to that of a larger scale device (data point at $w = 500$ μm). This demonstrates that a depletion layer, if present, is very small and does not influence substantially the properties of the 2DES.

The devices realized in this work are tunable using electric field effect. Red diamonds in figure 3(a) show the R_{sheet} versus gate voltage V_g behavior for a Dayem bridge. The gate voltage V_g was applied to an electrode placed on the back of the STO substrate (back gate configuration). After a first sweep of the gate voltage to positive values (the so called 'forming' process —not shown [39–41]), the R_{sheet} versus V_g curve is perfectly reproducible. A change of more than 2 orders of magnitude in the R_{sheet} can be obtained with a change of V_g of 40 V, similar

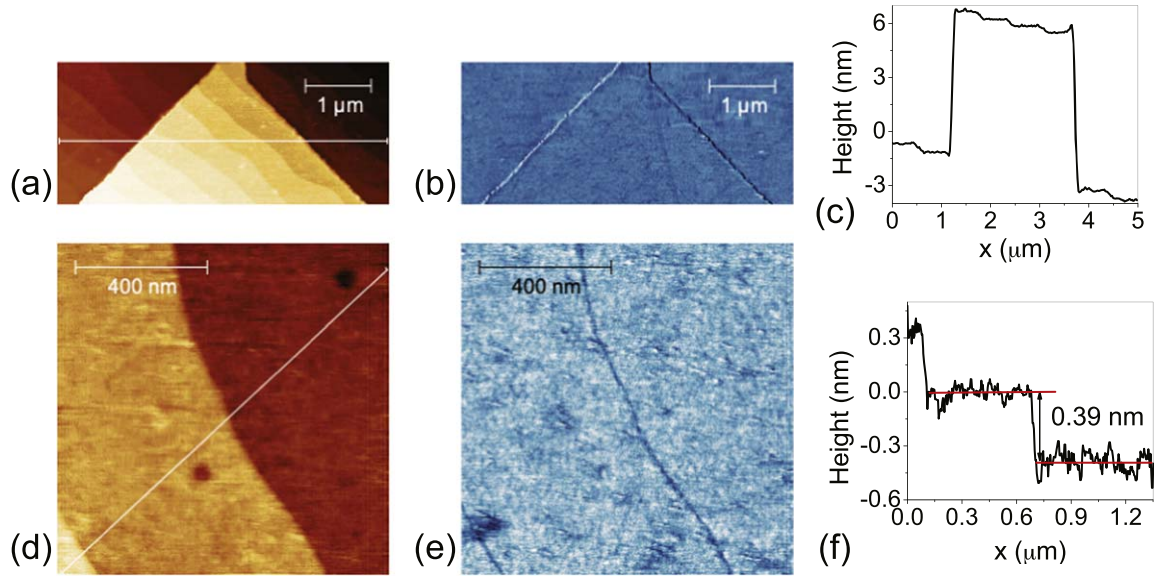


Figure 2. Upper panels: topography (a) and lateral force (b) across an etched Dayem bridge device. The images were acquired in contact mode. Panel (c) shows the profile along the white line depicted in the topography image (a). Bottom panels: topography (d) and lateral force (e) images on a small area of the ion-milled STO substrate showing two terraces with step height of one unit cell, as reported in panel (f). Lateral force shows that consecutive terraces have the same surface termination, as no contrast in the image is observed. Small changes in the lateral force signal are due to localized defects on the surface.

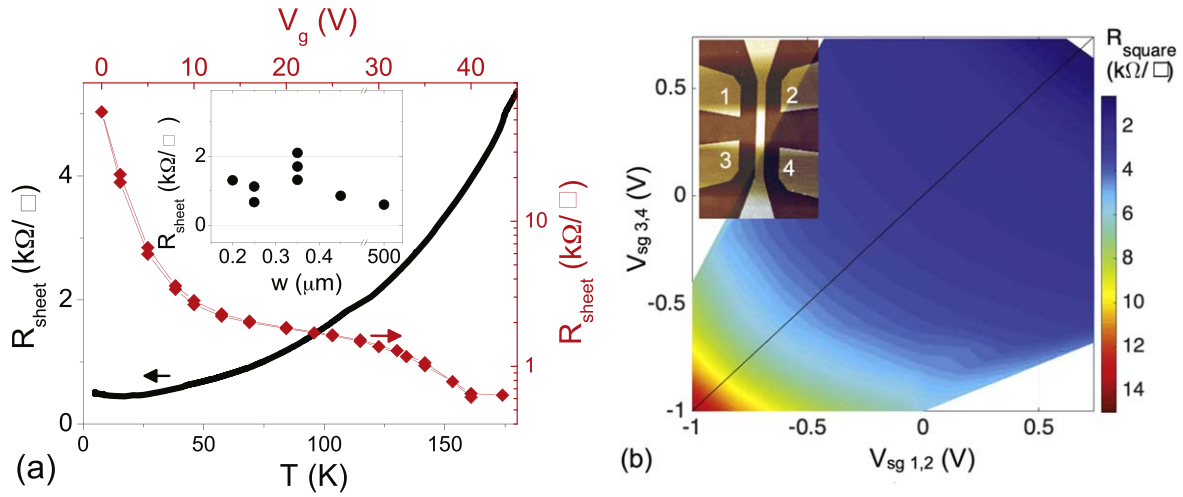


Figure 3. (a) Temperature (black data) and back gate voltage V_g (red data) dependence of R_{sheet} for a Dayem bridge with $w = 200$ nm and $L = 160$ nm. The R_{sheet} versus V_g data were obtained at 4.2 K. In the inset, we show the R_{sheet} at 4.2 K of devices of different width, ranging from 0.2 to 0.45 μm. The length of these devices ranges from 0.16 to 4 μm. We report also data from a 500 × 500 μm Hall bar device realized via photolithography and low temperature ion milling. (b) R_{sheet} of a side gate device 2S as a function of gate voltages applied independently to the two pairs of gate electrodes (see sketch in the inset) measured at 4.2 K. In black we show the $V_{g1,2} = V_{g3,4}$ line as a guide to the eye.

to that obtained for LAO/STO Dayem bridges realized with the amorphous template technique [26]. In the case of side gate devices the gate voltage can be applied also using the lateral electrodes. In figure 3(b) we show a contour map of the R_{sheet} of a device with geometry 2S (width $w = 450$ nm and length $L = 4$ μm). The width of the side gate electrodes (distance h in figure 1(e)) is 1.2 μm, their distance from the center of the channel (t) is 0.75 μm and the distance between the two side gates in the point closer to the channel (d) is 1 μm. To realize this plot, different values of gate voltages were applied independently to the two pairs of electrodes 1–2 and 3–4 (see inset in the same panel) in order to tune half of the channel length at a time. From the symmetry of the plot we can conclude that the two sections of the channel can be tuned independently and that the channel is remarkably uniform and homogeneous along its 4 μm length. During these measurements, the leakage current was stable below 2 nA, ensuring that the side electrodes are properly insulated from the central channel and that the STO substrate kept its insulating nature after the ion-milling process.

In figure 4(a) we show the carrier concentration measured on a Hall bar device (500 × 500 μm^2) realized with photolithography and low temperature ion milling. At $T = 5$ K we

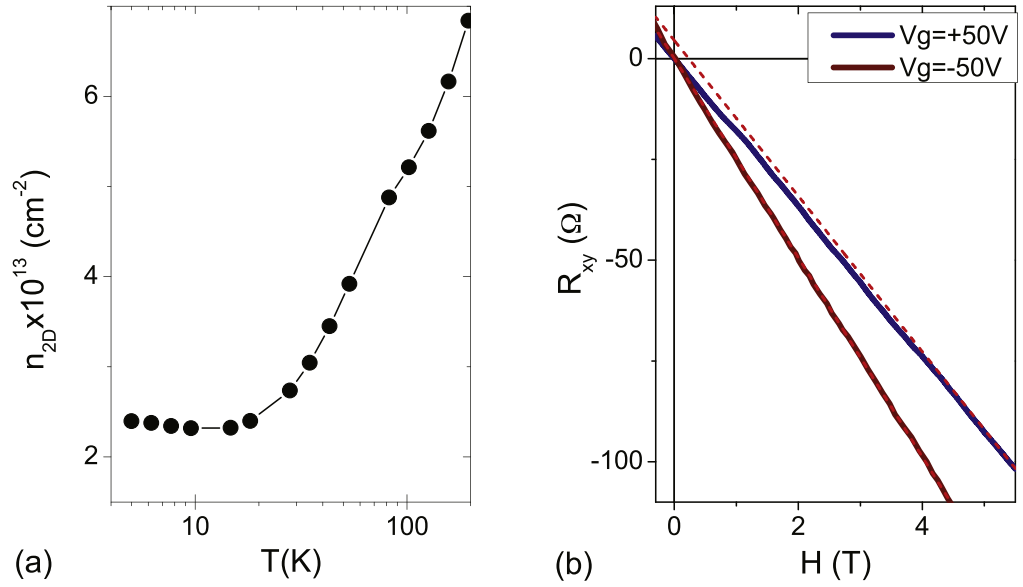


Figure 4. (a) Carrier concentration measured as a function of the temperature at $V_g = 0$. (b) Transverse resistance R_{xy} measured at $V_g = -50$ V (brown line) and $V_g = +50$ V (blue line) at $T = 5$ K in perpendicular magnetic field. The red dashed lines are fit around $H = 5$ T, highlighting the presence of a low field curvature at high gate voltage. The data in both panels were measured on large scale Hall bars realized using low temperature ion-milling.

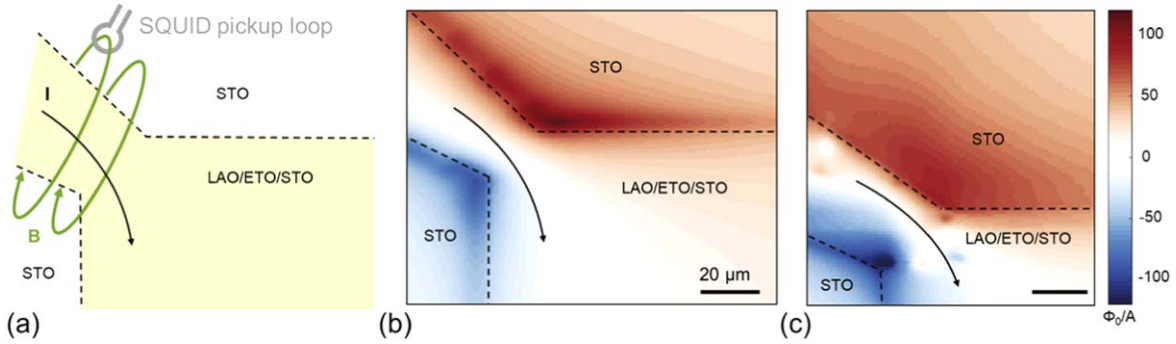


Figure 5. (a) Schematic of scanning SQUID pickup loop capturing field lines near the surface of a current carrying device. In this picture, the device area is shown in yellow color, while the substrate areas are shown in white. Dashed line marks the physical edge of the device. (b) Simulation of the magnetic flux pattern in a homogeneous conductor with the same geometry as the measured LAO/ETO/STO device. (c) Scanning SQUID data over a patterned LAO/ETO/STO device taken at 4 K. Dipole-shaped distortions to the image indicate regions with reduced conductivity.

measure $n_{2D} = 2.3 \times 10^{13}$ cm^{-2}, in excellent agreement with data reported in literature for pristine LAO/STO and LAO/ETO/STO samples [2, 42, 43]. Panel (b) shows the transverse resistance R_{xy} measured at $T = 5$ K for different values of the gate voltage. We observe that at high gate voltage, the data show a nonlinear behavior at low field ($H \sim 2$ T). It can be attributed to anomalous Hall effect taking place in ferromagnetic systems characterized by an intermediate/low carrier density and a non-negligible spin–orbit coupling, as previously reported for LAO/ETO/STO heterostructures [4, 43]. This result demonstrates that ferromagnetic properties are retained in patterned structures, with the same characteristics found in pristine samples.

Finally, we used a scanning SQUID microscopy to map the spatial distribution of current flow in patterned LAO/ETO/STO devices. The SQUID pickup loop captures the magnetic field lines generated by the current driven through the sample, as a function of location [44] (figure 5(a)). The current produces circulating magnetic fields around the sample. In a homogeneous sample the map shows positive (red) and negative (blue) field lines at the edges of the pattern, and a smooth flux profile inside the current carrying areas, as shown in the simulation of figure 5(b). Local distortions in the map of magnetic flux, for example dipoles or line features, point to the presence of defects, which could be localized regions, sometimes resolution limited, or elongated features [45]. These defects (regions with reduced or enhanced conductivity) distort the flow of current and therefore the distribution of magnetic field lines. Localized regions of reduced conductivity appear as a dipole-shaped signal in the raw data, reflecting the size of the defect, the shape of the sensor and the scan height. The data in figure 5(c) demonstrate that the patterned LAO/ETO/STO device presents homogeneous flow interrupted only by a few regions with reduced conductivity (likely related to defects in

the thin films), while the exposed STO areas show no indication of current carrying paths.

4. Conclusions

In this work we presented a fabrication technique based on low-temperature ion-milling for the realization of oxide 2DES complex nanodevices. This 'top down' approach involves a lithography step followed by an ion milling process where the sample is kept at low temperature, close to that of liquid nitrogen. The devices realized are stable over time and multiple thermal cycling between room and cryogenic temperatures. By a careful selection of the e-beam resist type and thickness, we realized nanodevices with dimensions down to 160 nm and properties comparable to that of pristine films. The strong tunability of the resistance of side gate devices demonstrates that no current paths are present in the etched STO areas between the nanochannels and the lateral electrodes, therefore the STO substrate keeps its insulating properties after the ion-milling process. The carrier concentration in the devices realized is comparable to that typically found in LAO/STO and LAO/ETO/STO 2DES. Scanning SQUID images confirm that no current flow outside the patterned areas, supporting the above conclusions.

The technique we present can be applied to all types of oxide heterostructures. In the present configuration, we estimate that an oxide thickness of maximum 10 nm can be etched before damaging the resist nanopattern. However, by resorting to a more robust e-beam resist this limit could probably be raised. Being a 'top down' approach, this technique does not involve manipulation of the substrate before thin films deposition, therefore it is particularly useful for the patterning of interfacial systems where termination and cleanliness of the substrate are of great importance. The formation of a LAO/ETO/STO 2DES is one of these cases: even a small amount of contaminants on the substrate could hamper the 2 u.c. ETO layer formation, resulting in an insulating LAO/ETO/STO interface. Furthermore, the technique we describe can be applied to a pre-tested heterostructure, increasing the yield of the nanofabrication procedure.

An important innovation our technique brings is also to expose the lateral sides of the devices, with little or no damage to the lateral areas of the system, giving the possibility to access the oxide 2DES from the side. This opens the way to the realization of hybrid normal/superconductor structures or even to superconductor/superconductor structures, where the 2DES could be proximized by another superconducting material. Adding the ferromagnetic properties of our LAO/ETO/STO heterostructures, many other exciting perspectives for a new class of hybrid devices can be envisaged.

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Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

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